

Hybrid Integration of Graphene Analog and Silicon Complementary Metal–Oxide–Semiconductor Digital Circuits

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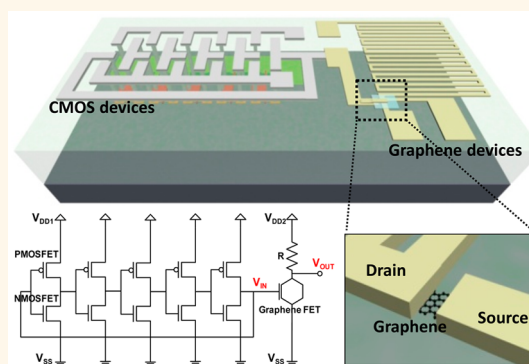
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S Supporting Information

ABSTRACT: We demonstrate a hybrid integration of a graphene-based analog circuit and a silicon-based digital circuit in order to exploit the strengths of both graphene and silicon devices. This mixed signal circuit integration was achieved using a three-dimensional (3-D) integration technique where a graphene FET multimode phase shifter is fabricated on top of a silicon complementary metal–oxide–semiconductor field-effect transistor (CMOS FET) ring oscillator. The process integration scheme presented here is compatible with the conventional silicon CMOS process, and thus the graphene circuit can successfully be integrated on current semiconductor technology platforms for various applications. This 3-D integration technique allows us to take advantage of graphene's excellent inherent properties and the maturity of current silicon CMOS technology for future electronics.

KEYWORDS: graphene, transistor, CMOS, hybrid, integrated, circuit



Graphene FETs have been extensively studied in recent years as candidates for next generation electronic devices.^{1–6} Recently, however, there seems to be consensus that graphene FETs are not suitable for digital circuits because of the absence of a bandgap in graphene. Nevertheless, graphene FETs still have strong advantages in analog applications due to their high carrier mobility and high saturation velocity.^{7–10} If graphene FETs can be integrated together with silicon complementary metal–oxide–semiconductor (CMOS) circuits for analog–digital mixed signal circuits on a single wafer, it will be possible to exploit the advantages of both graphene and silicon. We should be aware that large-scale integration using graphene is not easy because of the lack of availability of electronic quality graphene with reasonably high uniformity and low defect density required for large-scale integration of transistors.^{11–19} On the other hand, in contrast with digital circuits, analog circuits usually do not require such large-scale integration. Therefore, fabricating digital circuits using silicon CMOS and analog circuits using a graphene FET is potentially an ideal approach for a mixed signal integrated circuit (IC).^{20–23} In order to realize hybrid integration of silicon CMOS and a graphene FET, process compatibility should be considered because many of the graphene FET fabrication steps such as the graphene transfer process are not compatible with the silicon CMOS front-end process line.^{24–27} Taking this into account, we present here a process scheme based on three-dimensional (3-D) integration

of silicon CMOS and a graphene FET. With this technique, we fabricate graphene FET circuits on top of silicon CMOS circuits rather than making them side-by-side. We can thereby avoid process incompatibility issues and fully utilize the advantages of both circuits. In order to demonstrate this idea, we fabricated a silicon CMOS ring oscillator in the first level and a graphene multimode phase shifter in the second level. The output signal of the silicon CMOS ring oscillator is vertically linked to the graphene multimode phase shifter. The process incompatibility issue is overcome by sequential fabrication flow, where all CMOS components are first built on a silicon wafer, followed by the formation of a passivation layer and vertical interconnection. The graphene transistors are built on the passivation layer at low temperature. This wafer scale 3-D integration scheme can also be applied to other 2-D materials to be integrated into silicon CMOS ICs, and it significantly reduces fabrication process complexities and avoids process incompatibility, while also preserving the inherent electrical performances of each devices.

RESULTS AND DISCUSSION

Figure 1a shows a simplified cross sectional schematic of 3-D integration of silicon CMOS and a graphene FET. The silicon

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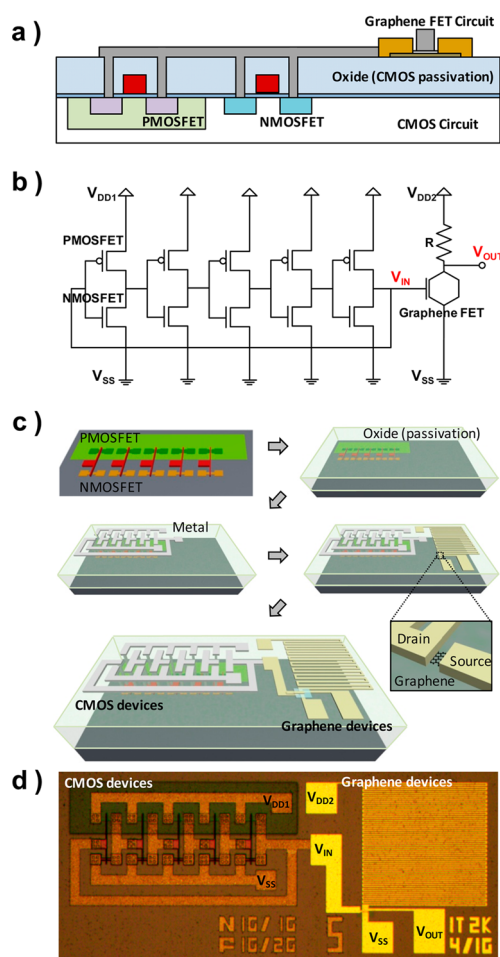


Figure 1. (a) Schematic drawing of cross section of graphene and CMOS hybrid-integrated circuit and (b) circuit diagram consisting of ring oscillator and phase shifter. (c) Schematic drawing of the CMOS-first and graphene-last process flow showing the integration method. A passivation layer of 400 nm SiO_2 was used to electrically separate the graphene phase shifter from the underlying silicon CMOS ring oscillator. (d) Optical microscope image of the actual hybrid-integrated circuit under test.

CMOS ring oscillator circuit in the first level is composed of an odd number of inverting stages, connected in a loop and powered by a direct current (DC) supply voltage. Its output, an alternating current (AC) signal, is vertically linked to the graphene multimode phase shifter. The gate electrode of the graphene FET is connected to a metal line *via* in the passivation layer. A circuit diagram consisting of the ring oscillator and the multimode phase shifter is shown in Figure 1b. A schematic 3-D drawing of the fabrication process steps is shown in Figure 1c, and an optical microscope image of the completed actual hybrid IC is presented in Figure 1d. Details of the fabrication can be found in the Methods section and Figure S1.

The output signal of the ring oscillator consisting of 13 inverting stages is plotted in Figure 2a, demonstrating the successful realization of silicon CMOS. Figure 2b shows that the number of inverting stages is inversely proportional to the oscillation frequency, while linearly proportional to the output peak to peak voltage (V_{pp}). When the ring oscillator has 13 stages, the output V_{pp} was 0.62 V, and the oscillation frequency was 233 kHz at $V_{DD} = 5$ V. The electrical characteristics of a unit transistor and the output signal of each ring oscillator are shown in Figures S2 and S3. The graphene multimode phase shifters were realized using a resistive-load and complementary push–pull configuration. Figure 2c,d presents transfer characteristics of a unit graphene FET, and Figure 2e,f presents output characteristics of multimode phase shifters, respectively. The shifters were successfully operated with am-bipolar characteristics, and thus the operation mode can be selected by controlling the input voltage (V_{IN}), as described in section S3 in Supporting Information.

We show that the graphene phase-shift has multimode operation, depending on the relationship between V_{IN} and the output voltage (V_{OUT}). In each mode, the circuit exhibits different performance in terms of the voltage gain, frequency response, and phase shifting. However, it should be noted that the relationship $V_{OUT} = V_{DD2} - I_{OUT}R_{LOAD}$ must always be satisfied in any case. Figure 3a shows the circuit diagram of the resistive-load configuration and the V_{OUT} – V_{IN} transfer characteristics at $V_{DD2} = 1$ V. When $V_{IN} < V_{MAX}$, which corresponds to mode 1 in Figure 3a, the graphene circuit is biased at the left branch of the conduction curve where the hole conduction

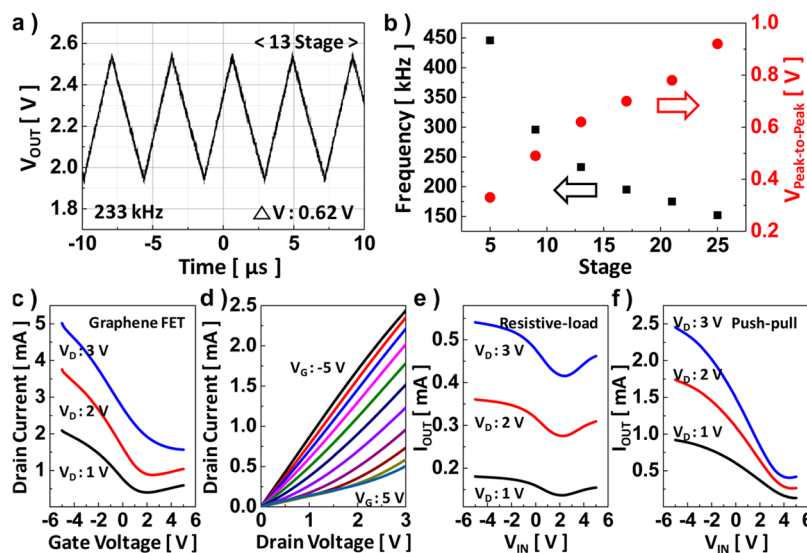


Figure 2. (a) CMOS oscillator output signal with 13 inverting stages at $V_{DD} = 5$ V. (b) Oscillator output frequency and peak-to-peak voltage (V_{pp}) as a function of the number of inverting stages. (c) I_D – V_G characteristics at $V_D = 1$ to 3 V and (d) I_D – V_D characteristics at $V_G = -5$ to 5 V of the single graphene transistor. (e) The resistive-load and (f) complementary push–pull characteristics for different graphene circuits and drain voltage.

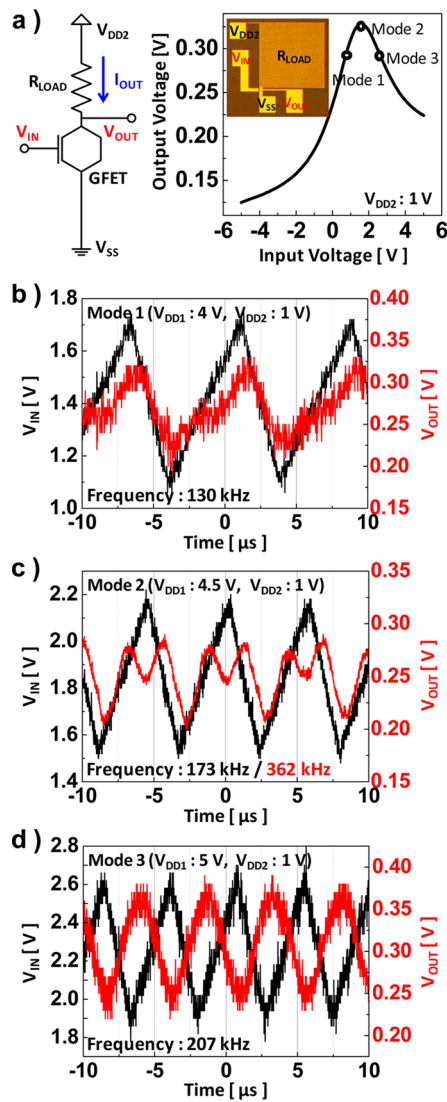


Figure 3. (a) Schematic for the triple mode single graphene transistor using a load resistor and its V_{OUT} – V_{IN} characteristics. The three dots represent three representative input voltages for the three different operation modes. (b) V_{OUT} has the same frequency and phase as V_{IN} when the circuit is biased at the left branch of the ambipolar I_D – V_G curve graphene transistor. (c) The circuit is in the frequency doubler mode when the circuit is biased near the Dirac point of the graphene transistor. (d) When the circuit is biased at the right branch of the ambipolar curve, V_{OUT} has the same frequency but a 180° phase shift compared to V_{IN} .

regime has negative transconductance. I_{OUT} decreases at the positive phase of the V_{IN} , resulting in a decrease of voltage drop across the load resistor and an increase of V_{OUT} . Similar to the positive phase of V_{IN} , V_{OUT} of the devices decreases at the negative phase of the V_{IN} , resulting in the same phases for both V_{IN} and V_{OUT} , which are presented in Figure 3b. V_{DD1} determines the bias condition to the silicon CMOS-based ring oscillator, while V_{DD2} determines that to the graphene multi-mode phase shifter. As the V_{IN} is the output of the silicon ring oscillator, adjusting V_{DD1} can control V_{IN} , while V_{DD2} remains constant. When $V_{IN} > V_{MAX}$, which corresponds to mode 3 in Figure 3a, the graphene circuit is biased at the right branch of the conduction curve where the electron conduction regime has positive transconductance. I_{OUT} of the devices increases at the positive phase of V_{IN} , resulting in an increase of the voltage

drop across the load resistor and thereby a decrease of the V_{OUT} . Thus, V_{OUT} exhibits a phase shift of 180° with respect to V_{IN} , as shown in Figure 3d. When V_{IN} is near V_{MAX} , which is represented as mode 2 in Figure 3a, the graphene circuit is biased at the minimum conduction point near the Dirac point. The oscillation of V_{IN} near the Dirac point causes oscillation of the operation mode between modes 1 and 3, resulting in frequency doubling of V_{OUT} , as shown in Figure 3c.

On the basis of a similar concept, the complementary push–pull structure using two graphene FETs is successfully demonstrated in Figure 4. V_{Dirac} of the top graphene FET (GFET2) is

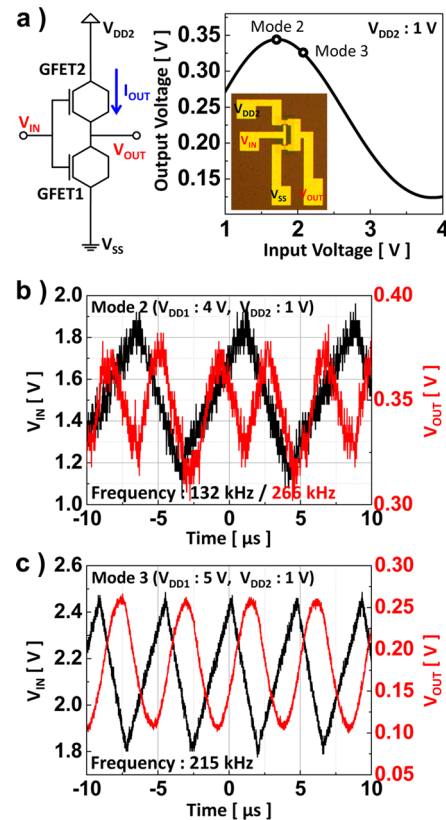


Figure 4. (a) Schematic for the complementary push–pull structure using two graphene transistors and its V_{OUT} – V_{IN} characteristics. The two dots represent two representative input voltages for the two different operation modes. (b) The circuit is in the frequency doubler mode when the circuit is biased near the Dirac point of the graphene driver transistor. The applied voltage is $V_{DD1} = 4$ V and $V_{DD2} = 1$ V, and the frequency of V_{IN} and V_{OUT} is 132 and 266 kHz. (c) When the circuit is biased at the right branch of the ambipolar curve of the graphene driver transistor, V_{OUT} has the same frequency but a 180° phase shift compared to V_{IN} .

larger than that of the bottom graphene FET (GFET1) because the drain potential in the channel of GFET2 is higher than that of GFET1. The operation voltage of the complementary push–pull is obtained between the Dirac voltages of the two GFETs, where the resistance of GFET2 increases and the resistance of GFET1 decreases with the increases of V_{IN} . This leads to a decrease of V_{OUT} as V_{IN} increases, as shown in Figure 4a. Similar to the resistive-load structure in mode 2 in Figure 3a, frequency doubling is clearly observed in Figure 4b when V_{IN} is near V_{MAX} , which is represented by mode 2 in Figure 4a. On the other hand, when $V_{IN} > V_{MAX}$, which is represented as mode 3 in Figure 4a, V_{OUT} exhibits a phase shift of 180° with respect to V_{IN} .

CONCLUSION

In summary, we successfully demonstrated 3-D integration of silicon CMOS and a graphene FET. A multimode phase shift was successfully operated, without using any external components outside the IC on the wafer. The mode of the graphene phase shift could be simply controlled by adjusting the bias voltage of the silicon CMOS circuit and that of the graphene inverter. This work demonstrates that graphene can be implemented on the platform of current silicon IC technology for various applications. This technique allows us to fully utilize the advantages of graphene's inherited excellent properties and the maturity of silicon technology for future electronics.

METHODS

The starting material of Si CMOS for the ring oscillator is a p-type silicon substrate of 1–10 $\Omega\cdot\text{cm}$ resistivity. The process flow is summarized in Figure S1. After standard precleaning, the wafer was oxidized in a wet ambient to grow a buffer oxide followed by deposition of LPCVD Si_3N_4 . Field oxide of 1 μm thickness was grown at 1100 $^\circ\text{C}$ for 140 min. The Si_3N_4 layer was subsequently removed using H_3PO_4 at 150 $^\circ\text{C}$ for 1 h. A p-well for the NMOS region was formed through boron implantation with a dose of $2 \times 10^{12} \text{ cm}^{-2}$ at 80 keV, covering the PMOS region with LPCVD SiO_2 . Similarly, an n-well for the PMOS region was formed through phosphorus implantation with a dose of $2 \times 10^{12} \text{ cm}^{-2}$ at 80 keV using the same sequence. A gate oxide of 30 nm thickness was grown through dry oxidation in both the NMOS and the PMOS regions after a sacrificial oxide was grown and removed for a high-quality gate oxide. The polysilicon gate electrode was deposited by LPCVD immediately after gate oxide growth to minimize undesired contamination on the gate oxide. A gate electrode was patterned using conventional lithography and a plasma etching process. The source/drain in the NMOS was formed by arsenic implantation with a dose of $5 \times 10^{15} \text{ cm}^{-2}$ and an energy of 50 keV, while that in the PMOS was formed by BF_3 implantation with a dose of $4 \times 10^{15} \text{ cm}^{-2}$ and an energy of 20 keV. The device geometries were $W/L = 10/10 \mu\text{m}$ for the NMOS and $20/10 \mu\text{m}$ for the PMOS, respectively.

A passivation oxide of 500 nm was deposited using LPCVD on top of the silicon transistors. A contact hole and aluminum metallization were used to make a bridge between the Si CMOS circuit at the first level and the graphene devices at the second level. The final alloy process was carried out in a 10% H_2 ambient at 400 $^\circ\text{C}$.

Synthesized graphene on the Cu film was transferred using PMMA on top of the passivation layer of Si CMOS. The transferred graphene layer was then annealed in a H_2 ambient at 400 $^\circ\text{C}$ for 30 min to remove residues on the graphene layers. An Au (50 nm)/Pd (10 nm) metal layer was deposited on graphene as a source/drain contact and then was patterned by a lift-off process. The device was then annealed in a vacuum ($\sim 1 \times 10^{-7}$ Torr) for 12 h to remove remaining adsorbates on graphene. A gate stack of Al_2O_3 (10 nm)/Au (50 nm) was deposited by atomic layer deposition followed by thermal evaporation. Graphene devices for multimode phase shifters were realized both in complementary push–pull and resistive-load configurations.

The push–pull configuration consisted of two graphene transistors with an inverter structure, while the resistive-load configuration consisted of one graphene transistor with an additional load resistor constructed between the V_{DD2} node and the drain of the graphene transistor. The resistive load was implemented with a bar resistance structure (width = 5 μm , length = 3.6 cm, and thickness = 50 nm) made of Au, the resistance of which is 4 k Ω . Two kinds of graphene multimode phase shifters were fabricated in order to demonstrate the versatility and feasibility achieved via the hybrid integration of Si CMOS ICs and graphene ICs. The resistive-load configuration consisting of a graphene FET and passive element showed a better trans-conductance value than the push–pull structure consisting of two GFETs. However, the latter was preferable in terms of device integration because the resistive load requires much larger area on the wafer.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b03382.

Details of process integration flow and characterization of MOSFET, ring oscillator, and graphene circuit (PDF)

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Notes

The authors declare no competing financial interest.

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